

ABSTRACT OF THE DISCLOSURE

A phase lock loop PLL which includes an oscillator having an oscillator signal whose frequency is related to a received error correction signal and phase frequency detector receiving and comparing the oscillator signal and a reference signal from a master circuit and generating the error correction signal based on the phase difference of the oscillator signal and the reference signal. A filter, including a capacitor, connects the error correction signal from the phase-frequency detector to the oscillator. A rate selector monitors a charge on the capacitor and controls the rate of error connection signals as a function of the charge on the capacitor.